Amendments to the Specification

Please delete paragraph [0027].

Please amend paragraph [0028] as follows:

[0028] FIG. 5 is a timing diagram illustrating signals provided by the components in FIGs. 3-4E[[F]];

Please amend paragraphs [0048] to [0050] as follows:

[0048] ~~FIG. 4F is an~~ An exemplary embodiment of a search data decoder and driver 340 ~~of~~ is shown in FIG. 3. Search data decoder and driver 340 receives an external search data (ext_search_data) signal, one clock signal on line 330, an internal search (int_search) signal generated by search control logic block 445 on line 335 and a mask register value (mask_reg_value) signal on line 325. The ext_search_data signal can be provided by the host processor (not shown). Search data decoder and driver ~~450~~ 340 outputs search lines SDx and SDy.

[0049] The components in FIGs. 4B – 4E[[F]] illustrate one way in which control signals for CAM device 300 could be obtained. Each component could be implemented with any suitable circuitry that provides the output signals in response to the input signals as described above. The illustrated components are only exemplary and other components could be used.

[0050] FIG. 5 is a timing diagram of several signals in CAM device 300. The clock signal acts as a control signal for the components in 4B – 4E[[F]] and other components. After CAM device 300 has been placed in test mode by a test signal to control block 430, control block 430 provides a test_en signal and the match lines of the CAM device are reset/disabled with a TM_ML_reset signal pulse from test control block 435. Control block 430 also provides a write enable (write_en) signal

pulse. In response, read/write decode logic block 440 decodes an address, illustratively Addr0, on the next rising edge of the clock signal and also provides a WL_0 pulse on the respective word line 132 at the next rising edge of the clock signal. By turning on transistor 405, the WL_0 pulse enables AND gate 425, allowing the signal ML on match line 130 to be gated to the priority encoder 355. In addition, an entry is written onto Addr0 during the write_en signal pulse.

Please amend paragraph [0061] as follows:

[0061] The circuitry and operations depicted in FIGs. 3 - 6 may be implemented in hardware, software, firmware, application specific integrated circuits (ASICs) field programmable gate arrays (FPGAs) or any suitable combination thereof. Specifically, CAM device 300, including all the circuitry in FIGs. 3 – 4E[[F]] may be implemented in a single integrated circuit.